Vivekananda College of Engineering & Technology, Puttur

[A Unit of Vivekananda Vidyavardhaka Sangha Puttur ®]

Affiliated to VTU, Belagavi & Approved by AICTE New Delhi

CRM08 Rev 1.10 CSE 16/10/2020

CONTINUOUS INTERNAL EVALUATION- 1

Dept:CSE	Sem / Div: 3/A&B	Sub:Computer Organization	S Code:18CS34		
Date:20/10/2020	Time: 2:30-4:00	Max Marks: 50	Elective:N		
Note: Answer any 2 full questions, choosing one full question from each part.					

-

Q N	Questions		RBT	COs		
11	PART A					
1 8	Describe the basic operational concepts between processor and memory.	10	L2	CO1		
l	Explain the basic instruction types with example	10	L2	CO1		
	How to measure the performance of a computer? Explain.	5	L3	CO1		
	OR					
2 8	Explain different types of addressing modes with example.	10	L2	CO1		
l	Explain various shift and rotate instruction with diagram and explain.	10	L2	CO1		
	With a memory layout starting at address "i" represent how "ABCD" data is stored in big endian and little endian assignment scheme in a system of word length 16 bits.		L3	CO1		
PART B						
3 8	With a neat diagram, explain the centralized arbitration and distributed bus arbitration scheme	10	L3	CO2		
ŀ	With supporting diagram; explain the following with respect to interrupts i)Interrupt Nesting ii)Simultaneous requests	10	L2	CO2		
	With neat diagrams, explain how to interface printer to the processor.	5	L2	CO2		
	OR					
4 8	With the help of timing diagram, briefly discuss the main phases of SCSI bus involved in its operation.	10	L3	CO2		
l	With a neat diagram, explain about how data is read in asynchronous bus scheme	10	L2	CO2		
	c Illustrate the tree structure of USB with diagram		L2	CO2		